Appl. No. 10/775,307
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In response to the Office Action dated August 24, 2005

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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (currently amended): A method for fabricating a multi-bit vertical memory cell, comprising:

providing a semiconductor substrate having a trench;

forming doped areas, acting as bit lines, in the semiconductor substrate near its surface and the bottom of the trench;

forming bit line insulating layers over each of the doping areas;

forming ~~a conformable oxide layer~~ an insulating layer over a sidewall of the trench and the bit line insulating layers to locally store electric charge; and

forming a conducting layer over the insulating layer and filling in the trench.

Claim 2 (original): The method for fabricating a multi-bit vertical memory cell of claim 1, a fabricating method of the doping areas further comprising:

forming a spacer over the sidewall of the trench;

performing ion implantation in the substrate using the spacer as a mask; and

removing the spacer.

Claim 3 (original): The method for fabricating a multi-bit vertical memory cell of claim 2, wherein the spacer is silicon nitride.

Claim 4 (original): The method for fabricating a multi-bit vertical memory cell of claim 2, wherein phosphorous ions are implanted.

Claim 5 (original): The method for fabricating a multi-bit vertical memory cell of claim 1, wherein the bit line insulating layers are formed by thermal oxidation.

Claim 6 (original): The method for fabricating a multi-bit vertical memory cell of claim 1, wherein the thicknesses of the bit line insulating layers are 300 to 2000Å.

Claim 7 (currently amended): The method for fabricating a multi-bit vertical memory cell of claim 1, wherein the ~~oxide layer~~ insulating layer is a silicon rich oxide layer.

Claim 8 (currently amended): The method for fabricating a multi-bit vertical memory cell of claim 1, wherein the thickness of the ~~oxide layer~~ insulating layer is 50 to 110Å.

Claim 9 (currently amended): The method for fabricating a multi-bit vertical memory cell of claim 1, further comprising a gate dielectric layer between the ~~oxide layer~~ insulating layer and the trench surface.

Claim 10 (original): The method for fabricating a multi-bit vertical memory cell of claim 9, wherein the gate dielectric layer is a gate oxide layer.

Claim 11 (original): The method for fabricating a multi-bit vertical memory cell of claim 9, wherein the thickness of the gate dielectric layer is 50Å.

Claim 12 (original): The method for fabricating a multi-bit vertical memory cell of claim 1, wherein the conducting layer is a poly layer.

Claims 13-20 (canceled)